SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MICROWIRE EEPROM COMMON I/O OPERATION

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SGS-THOMSON Microelectronics provides a wide range of serial access EEPROMs. The MICROWIRE® product line is designed for a 4-wire interface: SK the Clock input, CS the Chip Select Input, DI the Serial Data Input, and DO the Serial Data Output. Some MCUs such as the SGS-THOMSON Microcontroller series include a Serial Peripheral Interface (SPI) "on-chip", that can fit this MICROWIRE interface, but those EEPROMs can be used with any general purpose microcontroller where the interface wires are hooked to I/O ports or some equivalent circuitry.

Since DO output is in high impedance while instructions, addresses and data are shifted into the DI serial input, it seems attractive to tie DI and DO pins together to provide a common DI/DO bus. The chips can operate correctly in this configuration, provided that appropriate design rules are carefully followed. The possible troublesome situations are limited to the instructions where DO output is activated.

Such instructions include: READ,WRITE, ERASE, WRAL and ERAL.

This note reviews and details the specific points where precautions must be taken in common DI/DO applications.

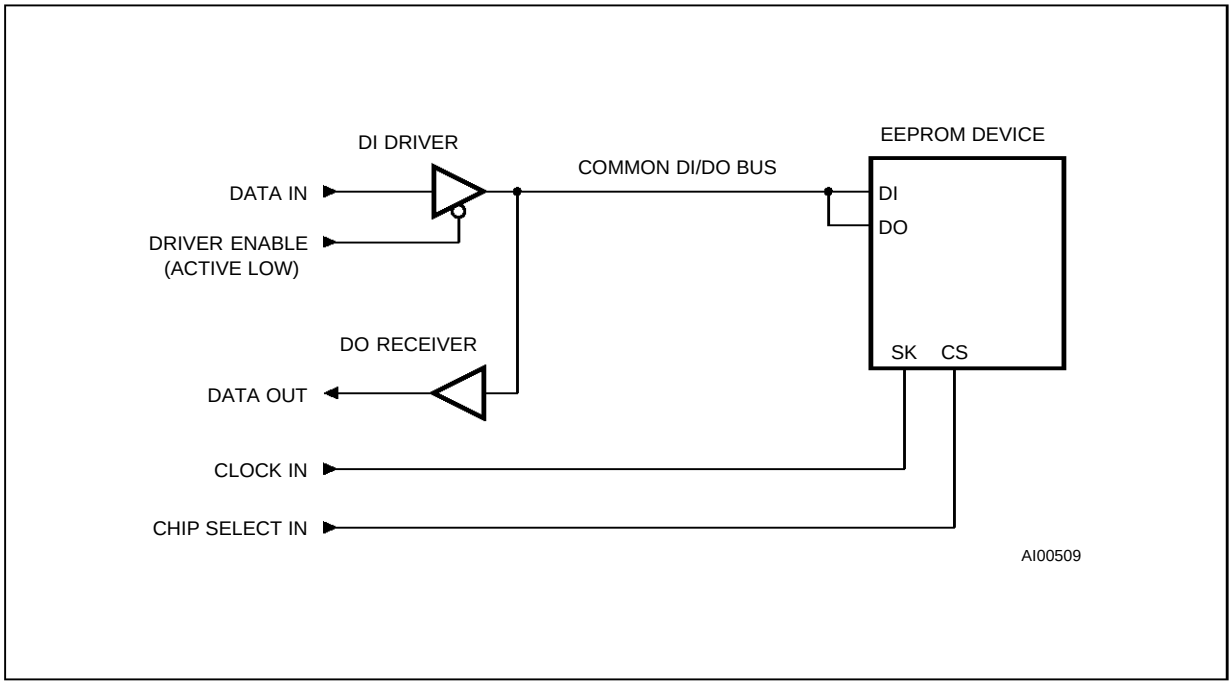
In order to provide the designer with a safe-design guide, all calculations are carried out upon the worst case values as specified in the data sheet of these EEPROM devices.

READ INSTRUCTION

Let's consider a typical common DI/DO application (as in Figure1). The DI driver and the DO receiver can be discrete logic or part of a microcontroller I/O port or any equivalent circuitry.

DO pin is in high impedance while the READ opcode and the address bits are clocked into the chip upon the rising edge of SK clock. These bits must be kept valid for a minimum hold time of t_{DIH}: see data sheet. However, upon the rising edge of SK where the last address bit (A0) is clocked into DI, the DO pin comes out of high impedance and outputs the leading bit (logical 0) which precedes the 16 bit data string (see example in Figure 2).

Figure 1. Typical Common DI/DO Application



The maximum delay between the rising edge of SK and the leading "0" bit is specified for a maximum of t_{PD0} (between 500 ns and 1µs, depending on the product); nevertheless, typical values of less than 100 ns can be found.
Since the DI driver must remain enabled with the A0 bit for a minimum of t_{DIH} (hold time) before being disabled, a bus conflict will occur if the A0 bit is a "1" (odd address registers). The consequences are:

– a low impedance path is created between V_{CC} and ground through DI driver and the on-chip DO

Figure 2. Read Instruction Example

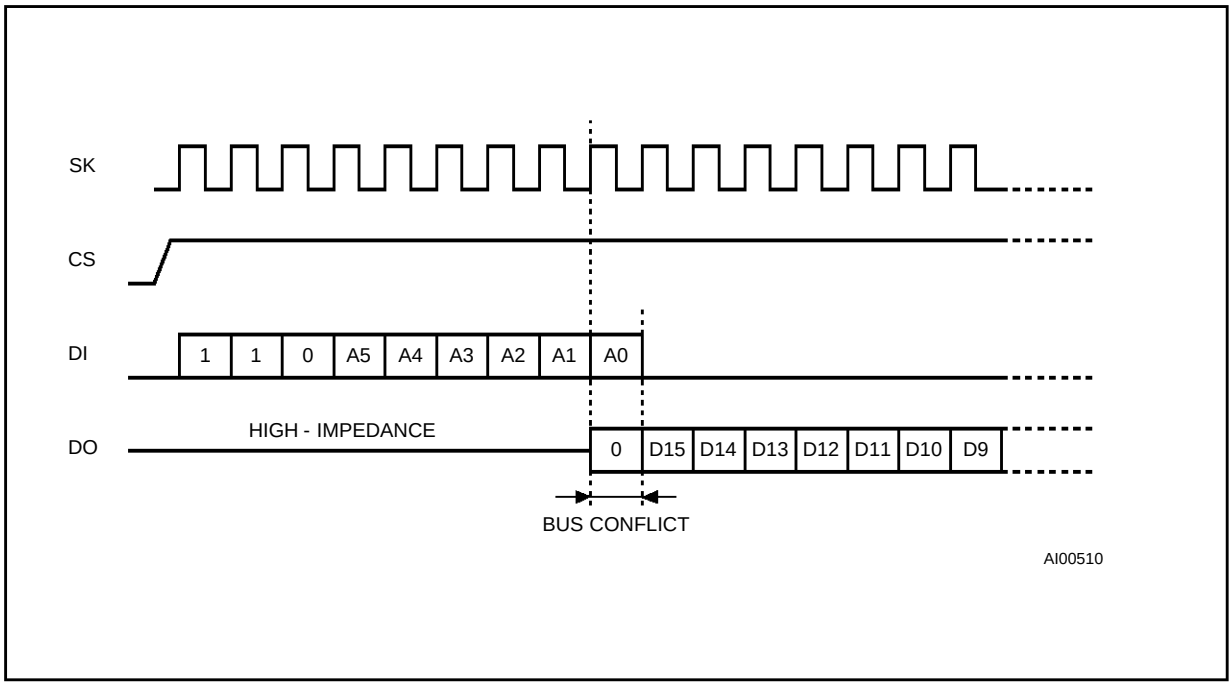
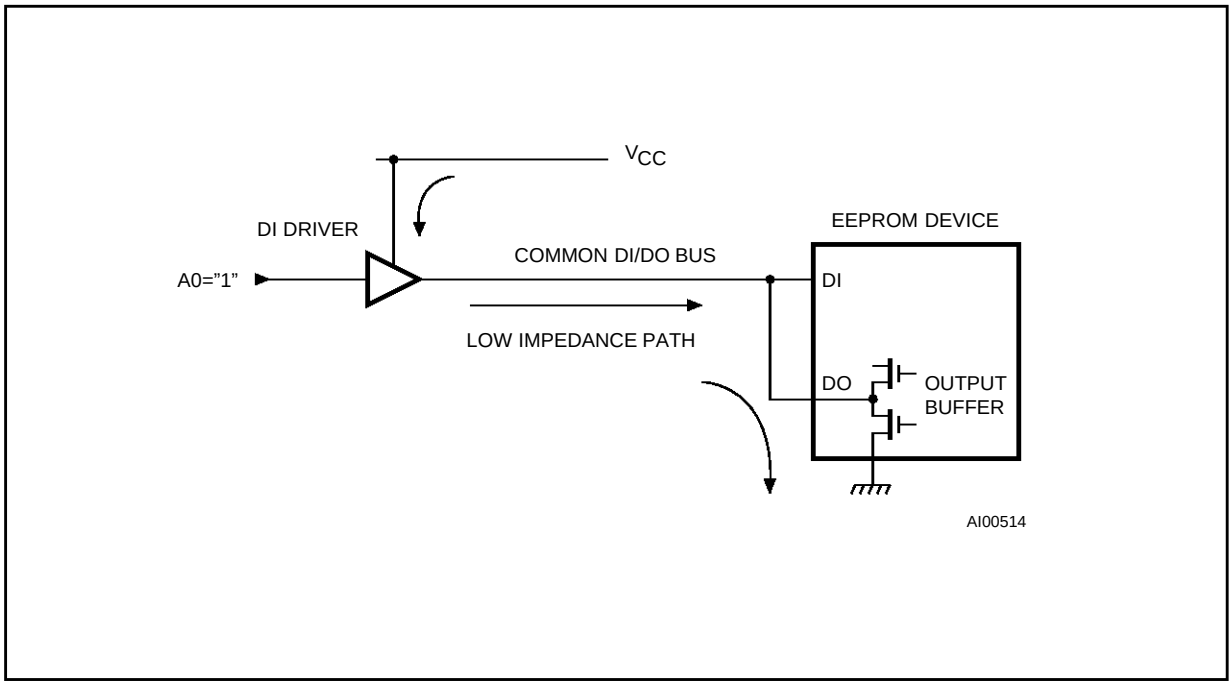


Figure 3. Short-Circuit between V_{CC} and Ground



output buffer (see Figure 3); this short-circuit may produce glitches on the power supply which can disturb all the circuits on the board;

– the logical level on the DI/DO bus is not well-defined as it is the result of the relative driving capability of the DI driver and the DO output buffer; the DI pin can even see a logical ”0” preventing the access of the odd address registers.

This trouble can be solved by inserting a current limiting resistor in the sinking current path. Figure 4 shows some possible locations for this resistor;

Figure 4. Possible Locations for the Current Limiting Resistor

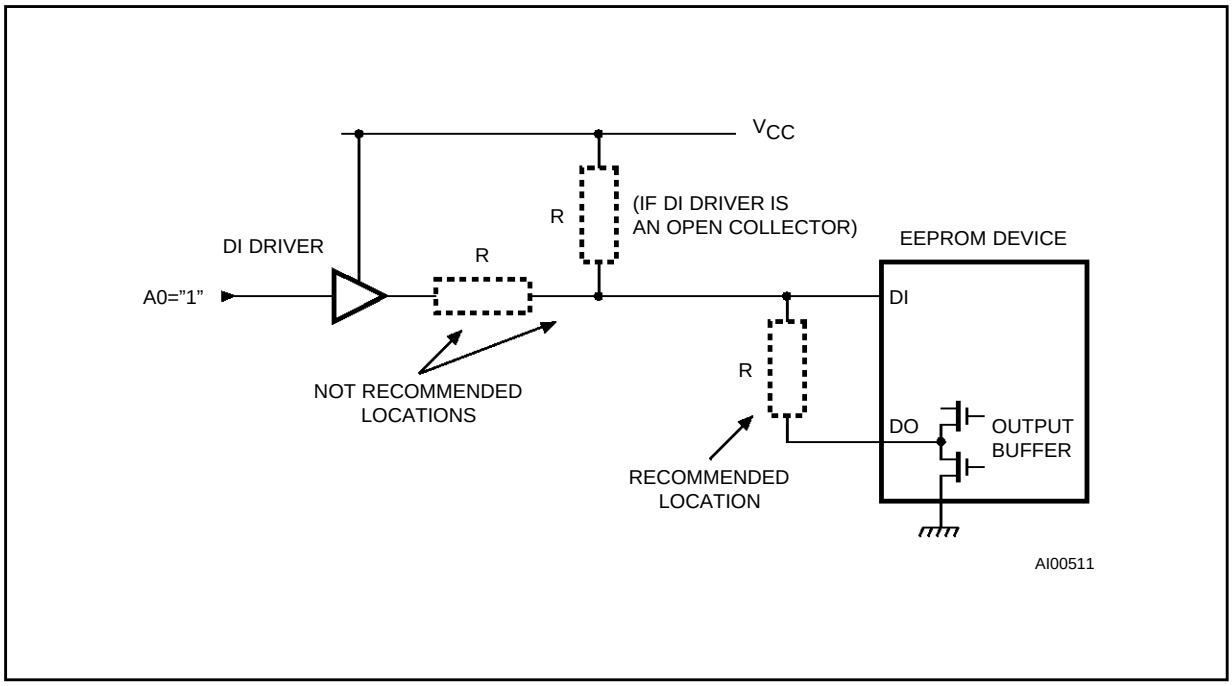
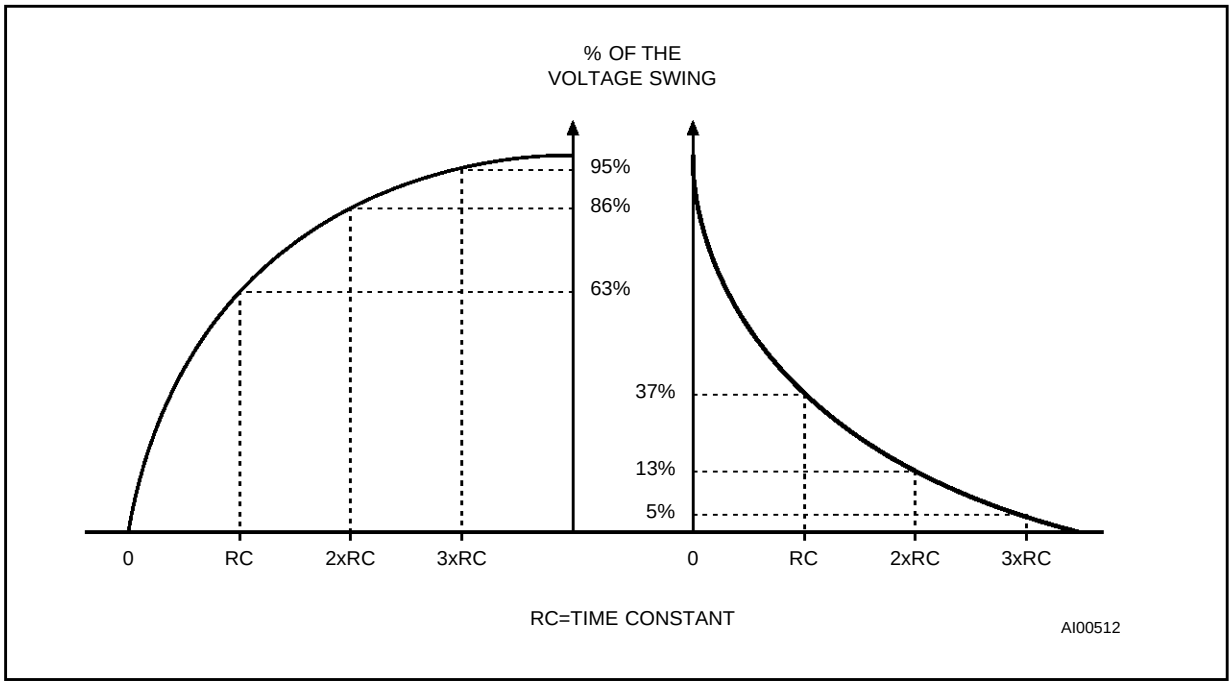


Figure 5. Exponential Charge and Discharge of the Bus Capacitance



however, the best location is between the DO output and the DI/DO bus for the following reasons:

– during the overlap time, the logical level on the DI/DO bus will be defined by the DI driver only, allowing the respect of the t_{DIH} hold time specification.

– as we discuss later, the R resistor slows down the propagation time of the DO output signals on the DI/DO bus, but only the 16 bits of data read from the chip are affected. If R were in series with the DI driver, all the input signals for all the instructions would be slowed down in the same way.

The R resistor doesn't have any effect as long as DO is in high impedance. During the execution of a READ instruction, R sinks some current from the DI driver during the short overlap time; then the DI driver is disabled and DO output takes control of the DI/DO bus through the R resistor.

Because of the bus capacitance C, the signals are distorded: the rising and falling edges of DO output are transformed into exponential curves whose shape depends on the time constant RC (see Figure 5).

The consequence is: after a rising edge of SK clock, the logical level on the DI/DO bus needs some delay before being considered as steadily established and ready to be sampled by the DO receiver. This safety delay can be estimated to be at least 3xRxC; after sampling, the subsequent rising edge of SK can occur.

When applying the results of Figure 5 to the worst case of DO output levels (see data sheet): V_{OH} min = 2.4 V, V_{OL} max = 0.4 V, Voltage Swing = 2 V, the DI/DO bus levels will be:

– logical "1" = 2.3 V minimum for a delay of 3xRC

– logical "0" = 0.5 V maximum after SK rising edge

It will be necessary to reduce the SK clock frequency when and only when shifting the 16 bits of data out from the EEPROM. All other operations can be performed at the nominal clock rate.

This reduction is of course directly related to the RC time constant of the DI/DO bus. Figures 6, 7, 8 show some experimental examples replotted from the scope with different values of R and C.

In the last example, the maximum clock frequency is: 1 / 3xRC = 100 KHz, assuming that DI/DO bus is sampled by the DO receiver circuitry just before the rising edge of the SK clock.

Figure 6. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, RC = 1 µs

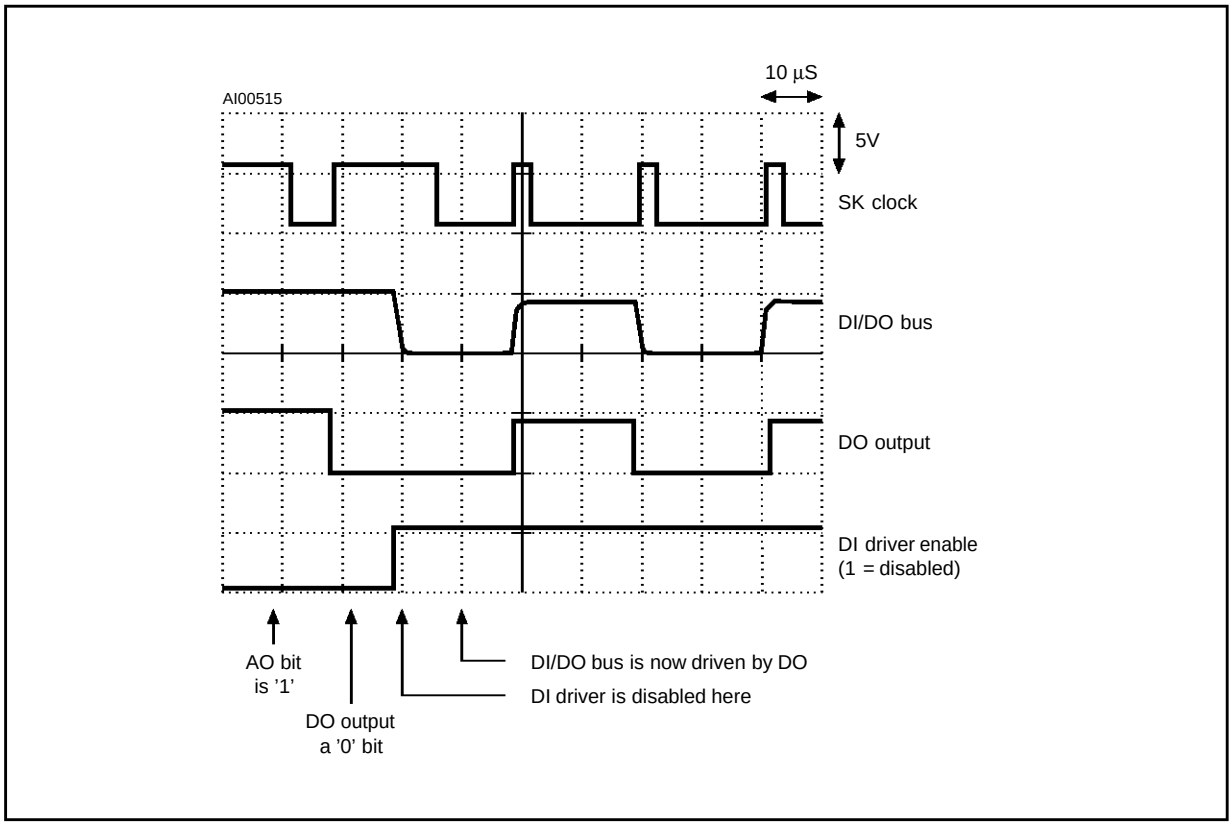


Figure 7. Oscilloscope Plot, R = 5 kΩ, C = 100 pF, RC = 500 ns

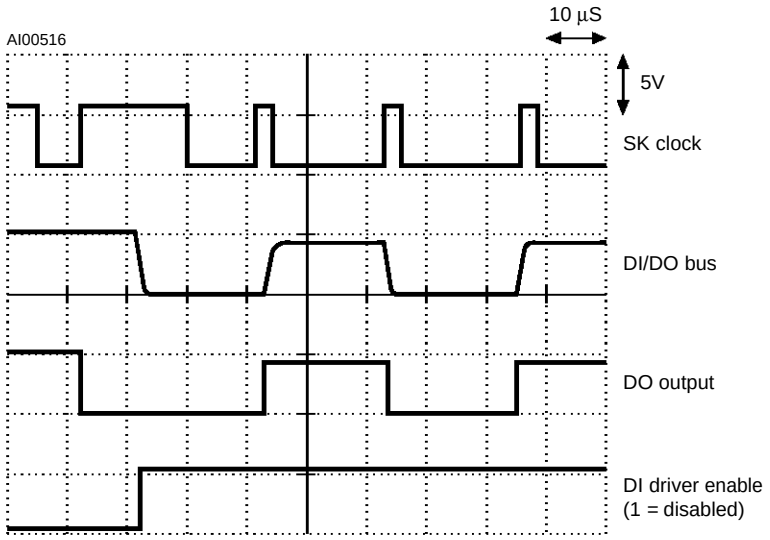
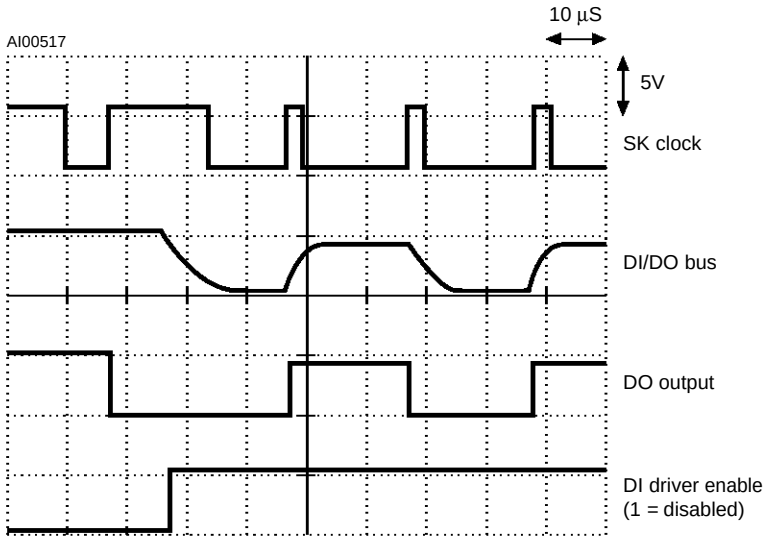


Figure 8. Oscilloscope Plot, R = 10 kΩ, C = 330 pF, RC = 3.3 µs



In order to avoid an important reduction of the clock frequency, the following techniques can be used which minimize the R and C values:

– to minimize the bus capacitance, it is important to implement the EEPROM device as close as possible to the DI driver/DO receiver circuitry for the shortest connection, and not share too many devices on the same DI/DO bus since the capacitance will be proportionnal to the number of devices connected in parallel to the same DI/DO bus.

– the value of the R resistor can be decreased as long as the DI driver can source the corresponding amount of current during the bus conflict time and as long as the power supply is adequately decoupled to withstand this transient of current. It's up to the designer to decide about the best trade-off based upon his specific application's requirements.

INTERFACE WITH CMOS CIRCUITS

The MICROWIRE EEPROM devices are specified for TTL compatible input/output levels; when using CMOS circuits to interface these devices, some precautions must be taken to ensure the correct interpretation of the logical levels.

Since the CMOS output-high levels are close to V_{CC} and output-low level close to 0V, it is obvious that there are no difficulties in driving the DI, CS and SK inputs of the EEPROM devices.

Concerning the DO output, the minimum output-high level is specified to 2.4 V, which is lower than the minimum input high level of CMOS (3.5 V for V_{CC} = 5 V). A common practice is to connect a pull-up resistor Rp between the DO output and V_{CC}, thus increasing the effective high-level in order to meet the CMOS specs.

Although this configuration suits perfectly to a separate DI and DO, it raises some difficulties in common DI/DO applications.

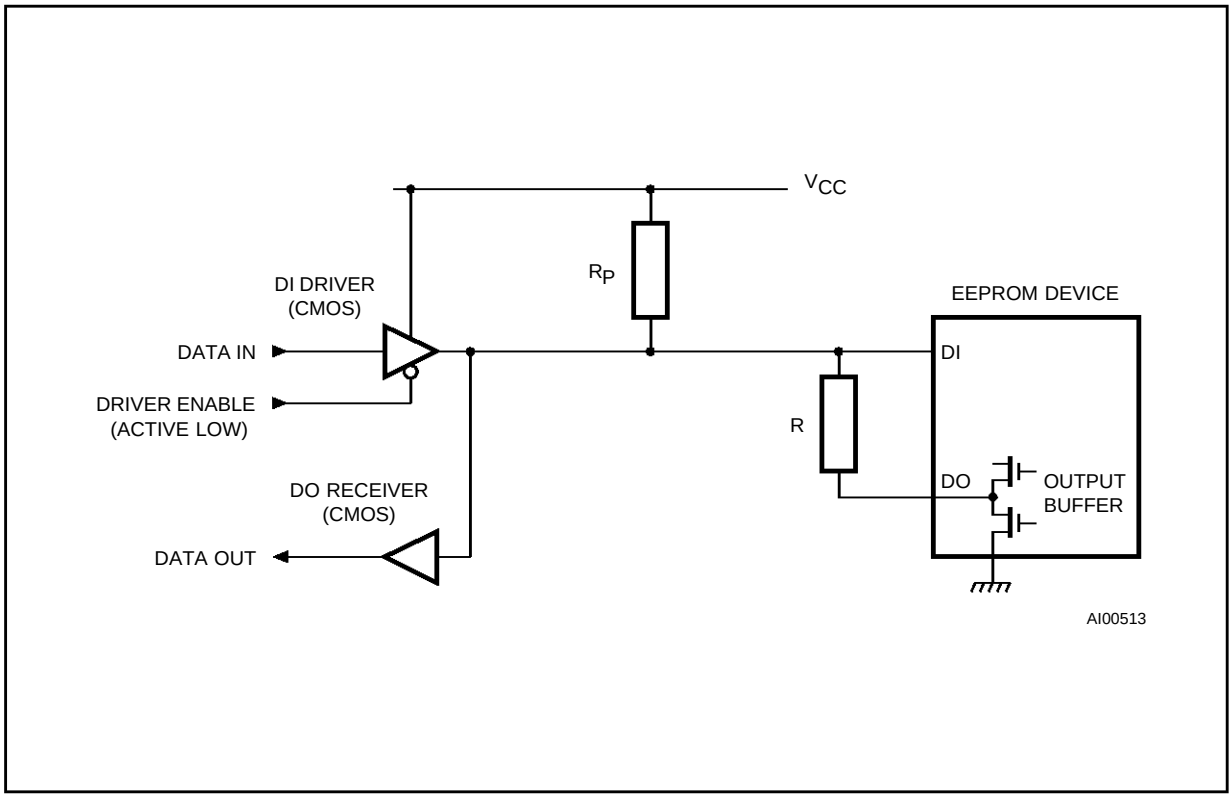
When DO output is a "zero" level, i.e. V_{OL}= 0.4 V, worst case conditions, the R and Rp resistors act together as a voltage divider on the DI/DO bus (see Figure 9); hence, the Rp resistor value must be at least 5 times greater than R value and the "zero" level on the DI/DO bus is:

$$0.4\ V + (5\ V - 0.4\ V) \times R / (R + Rp) = 1.17\ V$$

when Rp = 5xR

Although this value is 330 mV below the 1.5 V, maximum "zero" input level of CMOS, the wide

Figure 9. DI/DO Bus Configuration with Pull-up Resistor (Rp)



noise margin traditionally associated with CMOS is then significantly reduced.

For a ”1” to ”0” transition, the DO output on-chip buffer will have to discharge the bus capacitance through the R resistor and to sink some current from the V_{CC} through Rp resistor. In that case, we may see that the new time constant is equal to the product of the bus capacitance C with the parallel combination of R and Rp, which is 17% smaller than the one without Rp. However, the steady ”0” level is no more 0.4 V, as we assumed for TTL levels but 1.17 V as calculated above (if Rp = 5xR). Despite of this smaller time constant, the voltage swing between ”0” and ”1” is greater in this case (see later on); hence it is advised before sampling to keep the same ”rule of the thumb” delay of 3xRC after the SK clock rising edge.

The major problem is for the ”0” to ”1” transition. During a first step, the bus capacitance is charged through DO output in series with R and the Vcc power supply in series with Rp. These conditions lead to the same time constant as above (i.e. 17% smaller than the one without Rp).

But once the DI/DO bus voltage reaches the DO output level, the DO on-chip buffer is automatically turned off and the Rp resistor remains the only contributor to the charge of the bus capacitance, resulting into a much higher time constant: RpxC = 5xRxC (if Rp = 5xR).

If we consider the worst case ”1” output level for DO (V_{OH}= 2.4 V), it lasts a long time to go up to 3.5 V, which is the minimum ”1” input level for CMOS. It will last exactly 0.55xRpC (if Vcc = 5 V) or 2.75xRC after the DO output turn off, and we must add a reasonable noise margin (300 or 400 mV).

As a result: the minimum delay between the rising edge of SK and the sampling of the DI/DO bus should be 2 or 3 times longer than the one we’ve found for the TTL levels (without Rp), and the clock frequency must be reduced as much.
It is possible to avoid this situation by using a TTL level compatible input CMOS device such as the 74HCTXXX devices as DO receiver circuit, or a CMOS microcontroller that provides a ”TTL input levels” option on its I/O ports, such as the ST9 series, and thus get rid of this Rp resistor.

Figure 10. Oscilloscope Plot, R = 10 kΩ, C = 100 pF, Rp = 50 kΩ

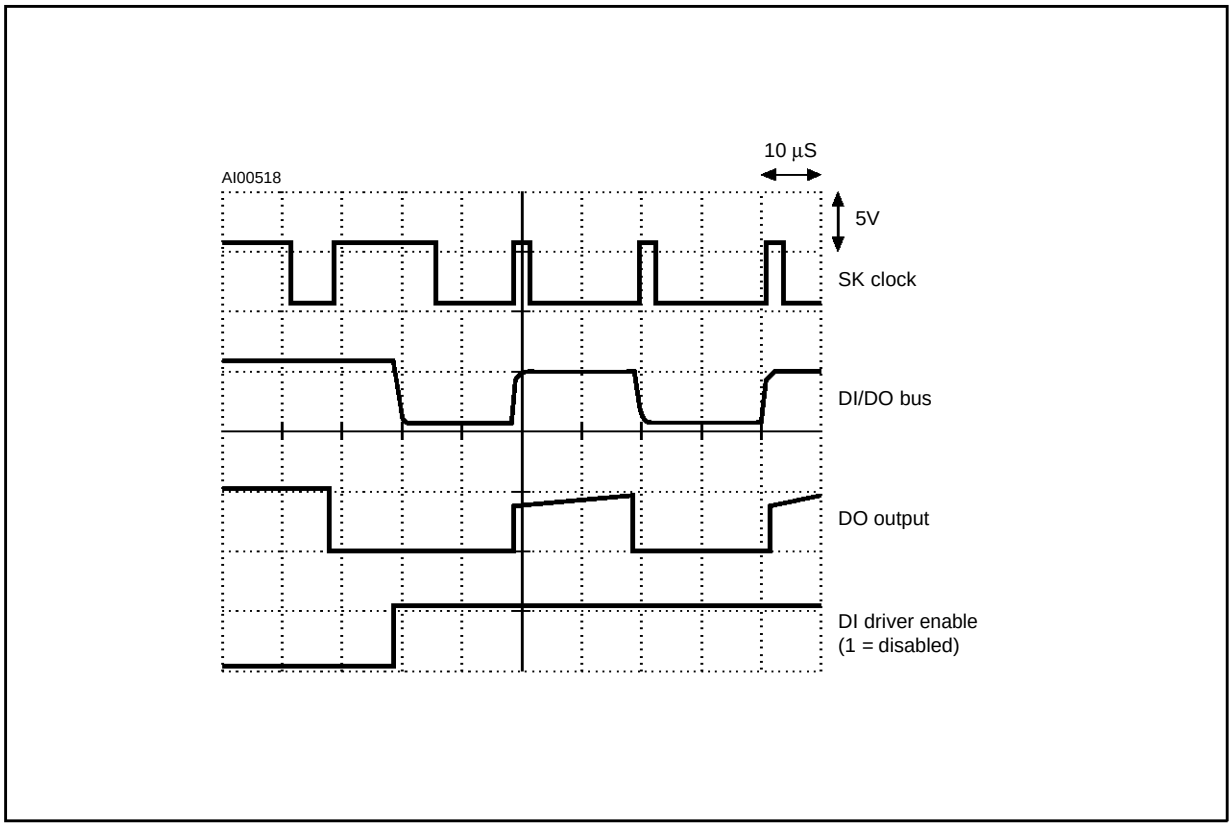
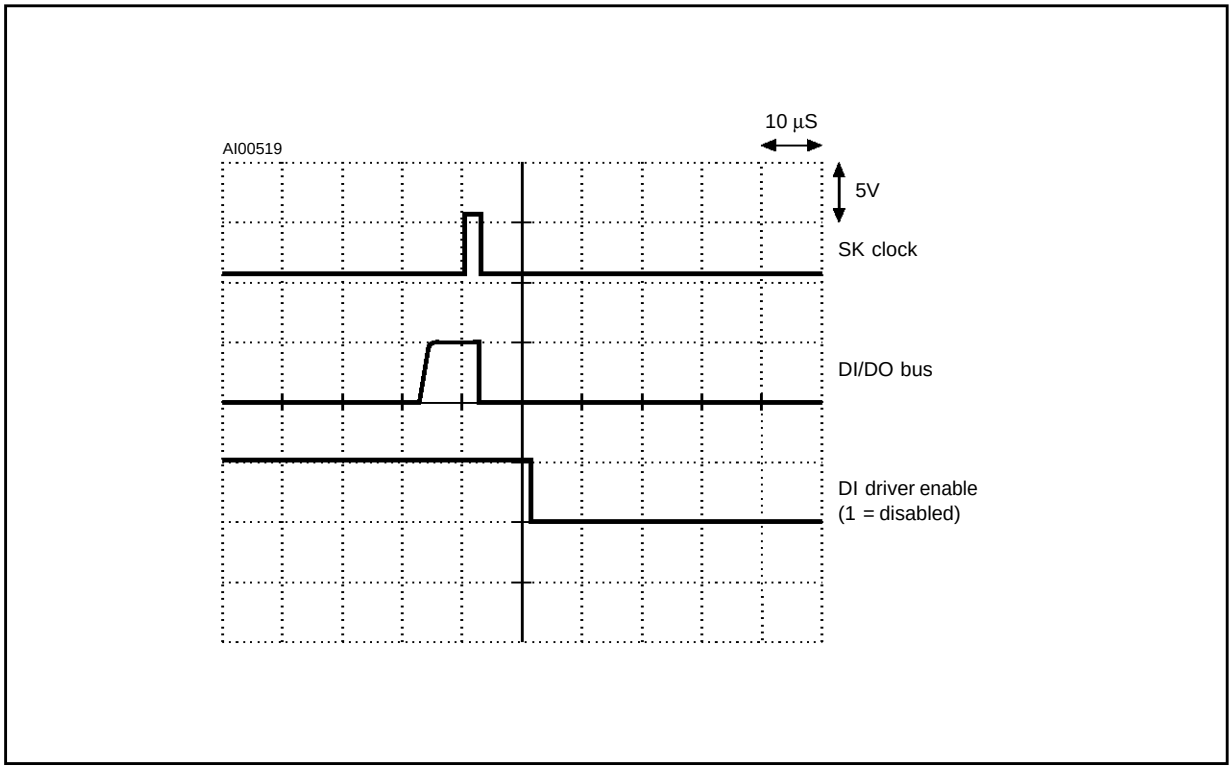


Figure 11. Acknowledge of the Ready/Busy Signal on DO Output



PROGRAMMING MODE: ACKNOWLEDGEMENT OF READY/BUSY STATUS

On the MICROWIRE EEPROM devices, the self-timed programming cycle uses DO output to indicate the ready/busy status of the chip.

The self-timed programming cycle begins with the falling edge of CS at the end of a programming instruction; such instructions include: WRITE, ERASE, WRAL and ERAL.

CS pin must be kept low for a minimum of t_{CS} (see data sheet). DO output remains in high impedance as long as CS is low; if CS is brougth high for clocking a new instruction, DO comes out of high impedance state and indicates the Ready/Busy status of the chip (0 = Busy, 1= Ready).

In common DI/DO applications, this may create again a bus conflict; therefore, it is recommended to cancel this status signal: this is very simply done by applying a single clock pulse on SK input while CS is high (see Figure 11).

The operation is scheduled as follows:

– shift into the chip a programming instruction
– bring CS low for t_{CS} minimum
– bring CS high
– monitor DI/DO bus till a ”1” level is detected (Ready)
– clock SK once
– bring CS low
– the chip is ready to accept a new instruction

It should also be noted that this Ready/Busy status can be found active after the power-up of the chip; therefore, it is recommended to clock SK once (with CS = 1) prior to any instruction.

CONCLUSION

This note gives some guidelines for the possibilities and the conditions of a safe operation in common DI/DO applications. The safety of these designs is based on the good safety margins and the worst case data sheet values used in the calculations. These calculations are of course not exhaustive, each designer may adapt them for any given application.